Introduction to Power MOSFETs and their Applications

INTRODUCTION

The Power MOSFETs that are available today perform the same function as Bipolar transistors except the former are voltage controlled in contrast to the current controlled Bipolar devices. Today MOSFETs owe their ever-increasing popularity to their high input impedance and to the fact that being a majority carrier device, they do not suffer from minority carrier storage time effects, thermal runaway, or second breakdown.

MOSFET OPERATION

An Understanding of the operation of MOSFETs can best be gleaned by the first considering the lateral N-channel MOSFET shown in Figure 1.

With no electrical bias applied to the gate G, no current can flow in either direction underneath the gate because there will always be a blocking PN junction. When the gate is forward biased with respect to the source S together with an applied drain-source voltage, as shown in Figure 2, the free hole carriers in the p-epitaxial layer are repelled away from the gate area creating a channel, which allows electrons to flow from the source to the drain. Note that since the holes have been repelled from the gate channel, the electrons are the “majority carriers” by default. This mode of operation is called “enhancement” but is easier to think of enhancement mode of operation as the device being “normally off”, i.e., the switch blocks the current until it receives a signal to turn on. The opposite is depletion mode, which is normally “on” device.

The advantages of the lateral MOSFET are:
1. Low gate signal power requirement. No gate current can flow into the gate after the small gate oxide capacitance has been charged.
2. Fast switching speeds because electrons can start to flow from drain to source as soon as the channel opens. The channel depth is proportional to the gate voltage and pinches closed as soon as the gate voltage is removed, so there is no storage time effect as occurs in transistors.
The major disadvantages are:
1. High resistance channels. In normal operation, the source is electrically connected to the substrate. With no gate bias, the depletion region extends out from the N+ drain in a pseudo-hemispherical shape. The channel length $L$ cannot be made shorter than the minimum depletion width required to support the rated voltage of the device.
2. Channel resistance may be decreased by creating wider channels but this is costly since it uses up valuable silicon real estate. It also slows down the switching speed of the device by increasing its gate capacitance.

Enter vertical MOSFETs!
The Power MOSFET structure (also known as DMOS) is shown Figure 3.

The current path is created by inverting the p-layer underneath the gate by the identical method in the lateral MOSFETs. Source current flows underneath this gate area and then vertically through the drain, spreading out as it flows down. A typical MOSFET consists of many thousands of N+ sources conducting in parallel. This vertical geometry makes possible lower on-state resistances ($R_{DS(on)}$) for the same blocking voltage and faster switching than the lateral MOSFETs.

There are many vertical construction designs possible, e.g., V-groove and U-groove, and many source geometries, e.g. squares, triangles, hexagons, etc. The many considerations that determine the source geometry are $R_{DS(on)}$, input capacitance, switching times and transconductance.

PARASITIC DIODE

Early versions of MOSFETs were susceptible to voltage breakdown due to voltage transients and also had a tendency to turn on under high rates of rise of drain-to-source voltage (dV/dt). Both resulted in catastrophic failures. The dV/dt turn-on was due to the inherent parasitic NPN transistor incorporated within the MOSFET, shown schematically in Figure 4a. Current flow needed to charge up junction capacitance $C_{DG}$ acts like base current to turn on the parasitic NPN.

The parasitic NPN action is suppressed by shorting the N+ source to the P+ body using the source metallization. This now creates an inherent PN diode anti-parallel to the MOSFET transistor (see Figure 4b). Because of its extensive junction area, the current ratings and thermal resistance of this diode exhibit a very long reverse recovery time and large reverse recovery current due to the long minority carrier lifetimes in the N-drain layer, which precludes the use of this
diodes except for very low frequency applications, e.g., motor control circuit shown in Figure 5. However in high frequency applications, the parasitic diode must be paralleled externally by an ultra-fast rectifier to ensure that the parasitic diode does not turn on. Allowing it to turn will substantially increase the device power dissipation due to the reverse recovery losses within the diode and also leads to higher voltage transients due to the larger reverse recovery current.

CONTROLLING THE MOSFET

A major advantage of the Power MOSFET is its very fast switching speeds. The drain current is strictly proportional to gate voltage so that the theoretically perfect device could switch in 50ps - 200ps, the time it takes the carriers to flow from source to drain. Since the MOSFET is a majority carrier device, a second reason why it can outperform the junction transistor is that its turn-off is not delayed by minority carrier storage time in the base. A MOSFET begins to turn off as soon as its gate voltage drops down to its threshold voltage.

SWITCHING BEHAVIOR

Figure 6 illustrates a simplified model for the parasitic capacitances of a Power MOSFET and switching voltage waveforms with a resistive load. There are several different phenomena occurring during turn-on. Referring to the same figure:
Time interval $t_1 < t < t_2$:

The initial turn-on delay time $t_{d(\text{ON})}$ is due to the length of time it takes $V_{GS}$ to rise exponentially to the threshold voltage $V_{GS(\text{TH})}$. From Figure 6, the time constant can be seen to be $R_S \times C_{GS}$.

Typical turn-on delay approximation is:

$$t_{d(\text{on})} = R_S \times C_S \times 1 \ln\left(1 - \frac{V_{GS(\text{min})}}{V_{PK}}\right)$$

(1)

Note that since the signal source impedance appears in the $t_d$ equation, it is very important to pay attention to the test conditions used in measuring switching times.

Physically one can only measure input capacitance $C_{iss}$, which consists of $C_{GS}$ in parallel with $C_{DG}$. Even though $C_{GS} >> C_{DG}$, the later capacitance undergoes a much larger voltage excursion so its effect on switching time cannot be neglected.

Plots of $C_{iss}$, $C_{oss}$, and $C_{rss}$ for the Fairchild Semiconductor Supersot$^\text{TM}$ NDS351N are shown in Figure 7 below. The charging and discharging of $C_{DG}$ is analogous to the “Miller” effect that was first discovered with electron tubes and dominates the next switching interval.
Time interval $t_2 < t < t_3$:

Since $V_{GS}$ has now achieved the threshold value, the MOSFET begins to draw increasing load current and $V_{DS}$ decreases. $C_{DG}$ must not only discharge but its capacitance value also increases since it is inversely proportional to $V_{DS}$, namely:

$$C_{DG} = \frac{C_{DG0}}{V_{DS}}$$  \hspace{1cm} (2)

Unless the gate driver can quickly supply the current required to discharged $C_{DG}$, voltage fall will be slowed with increases in turn-on time.

Time interval $t_3 < t < t_4$:

The MOSFET is now on so the gate voltage can rise to the overdrive level.

Turn-off interval $t_4 < t < t_6$:

Turn-off occurs in reverse order. $V_{GS}$ must drop back close to the threshold value before $R_{DS(on)}$ will start to increase. As $V_{DS}$ starts to rise, the Miller effect due to $C_{DG}$ re-occurs and impedes the rise of $V_{DS}$ as $C_{DG}$ recharges to $V_{CC}$.

Specific gate drive circuits for different applications are discussed and illustrated later in this paper.

**MOSFET CHARACTERIZATION**

The output characteristics ($I_D$ vs $V_{DS}$) of the Fairchild Semiconductor Supersot™ NDS351N are illustrated in Figures 8 and 9. The two distinct regions of operation in Figure 8 have been labeled “linear” and “saturated”. To understand the difference, recall that the actual current path in a MOSFET is horizontal through the channel created under the gate oxide and then vertical through the drain. In the linear region of operation, the voltage across the MOSFET channel is not sufficient for the carriers to reach their maximum current density. The static $R_{DS(on)}$, defined simply as $V_{DS}/I_{DS}$, is a constant.

As $V_{DS}$ is increased, the carriers reach their maximum drift velocity and the current amplitude cannot increase. Since the device is behaving like a current generator, it is said to have high output impedance. This is the so-called “saturation” regions. One should also note that in comparing MOSFET operation to Bipolar transistor, the linear and saturated regions are just the opposite to the MOSFET. The equal spacing between the output $I_D$ curves for constant step in $V_{GS}$ indicates that the transfer characteristics in Figure 9 will be linear in the saturated region.

![Figure 8. NDS351N Output Characteristics](image)

![Figure 9. NDS351N Transfer Characteristics](image)
IMPORTANCE OF THRESHOLD VOLTAGE

Threshold voltage $V_{GS(th)}$ is the minimum gate voltage that initiates drain current flow. $V_{GS(th)}$ can be easily measured on a Tektronix 576 curve tracer by connecting the gate to the drain and recording the required drain voltage for a specified drain current, typically 250µA. $V_{GS(th)}$ in Figure 9 is 1.6V. While a high value of $V_{GS(th)}$ can apparently lengthen turn-on delay time, a low value for Power MOSFET is undesirable for the following reasons:

1. $V_{GS(th)}$ decreases with increased temperature.
2. The high gate impedance of a MOSFET makes it susceptible to spurious turn-on due to gate noise.
3. One of the more common modes of failure is gate-oxide voltage punch-through. Low $V_{GS(th)}$ requires thinner oxides, which lowers the gate oxide voltage rating.

POWER MOSFET THERMAL MODEL

Like all other power semiconductor devices, MOSFETs operate at elevated junction temperature. It is important to observe their thermal limitations in order to achieve acceptable performance and reliability. Specification sheets contain information on maximum junction temperature ($T_{J(max)}$), safe operating areas, current ratings and electrical characteristics as a function of $T_J$ where applicable. However, since it is still not possible to cover all contingencies, it is still important that the designer perform some junction calculations to ensure that the device operates within specifications.

Figure 10 shows an elementary, steady-state, thermal model for any power semiconductor and the electrical analogue. The heat generated at the junction flows through the silicon pellet to the case or tab and then to the heat sink. The junction temperature rise above the surrounding environment is directly proportional to this heat flow and the junction-to-ambient thermal resistance. The following equation defined the steady-state thermal resistance $R_{θJA}$ between device junction to ambient:

$$R_{θJA} = \frac{T_J - T_A}{P} \tag{3}$$

where:
- $T_J$ = average temperature at the device junction (°C)
- $T_A$ = average temperature at ambient (°C)
- $P$ = average heat flow in watts (W).

Note that for thermal resistance to be meaningful, two temperature reference points must be specified. Units for $R_{θJA}$ are °C/W.
The thermal model shows symbolically the locations for the reference points of junction temperature, case temperature, sink temperature and ambient temperature. These temperature reference points define the following thermal resistances:

- $R_{\theta_{JC}}$: Junction-to-Case thermal resistance.
- $R_{\theta_{CS}}$: Case-to-Sink thermal resistance.
- $R_{\theta_{SA}}$: Sink-to-Ambient thermal resistance.

Since the thermal resistances are in series:

$$ R_{\theta_{JA}} = R_{\theta_{JC}} + R_{\theta_{CS}} + R_{\theta_{SA}} \quad (4) $$

The design and manufacture of the device determines $R_{\theta_{JC}}$ so that while $R_{\theta_{JC}}$ will vary somewhat from device to device, it is the SOLE RESPONSIBILITY of the manufacturer to guarantee a maximum value for $R_{\theta_{JC}}$. Both the user and manufacturer must cooperate in keeping $R_{\theta_{CS}}$ to an acceptable maximum. Finally, the user has sole responsibility for the external heat sinking.

By inspection of Figure 10, one can write an expression for $T_J$:

$$ T_J = T_A + P \times (R_{\theta_{JC}} + R_{\theta_{CS}} + R_{\theta_{SA}}) \quad (5) $$

While this appears to be a very simple formula, the major problem using it is due to the fact that the power dissipated by the MOSFET depends upon $T_J$. Consequently one must use either an iterative or graphical solution to find the maximum $R_{\theta_{SA}}$ to ensure stability. But an explanation of transient thermal resistance is in order to handle the case of pulsed applications.

Use of steady-state thermal resistance is not satisfactory for finding peak junction temperatures for pulsed applications. Plugging in the peak power value results in overestimating the actual junction temperature while using the average power value underestimates the peak junction temperature at the end of the power pulse. The reason for the discrepancy lies in the thermal capacity of the semiconductor and its housing, i.e., its ability to store heat and to cool down before the next pulse.

The modified thermal model for the MOSFET is shown in Figure 11. The normally distributed thermal capacitances have been lumped into single capacitors labeled $C_J$, $C_C$, and $C_S$. This simplification assumes current is evenly distributed across the silicon chip and that the only significant power losses occur in the junction. When a step pulse of heating power, $P$, is introduced at the junction, figure 12a shows that $T_J$ will rise at an exponential rate to some steady state value dependent upon the response of the thermal network. When the power input is terminated at time $t_2$, $T_J$ will decrease along the curve indicated by $T_{cool}$ in Figure 12a back to its initial value. Transient thermal resistance at time $t$ is thus defined as:

$$ Z_{\theta_{JC}} = \frac{\Delta T_{JC}(t)}{P} \quad (6) $$

The transient thermal resistance curve approaches the steady-state value at long times and the slope of the curve for short times is inversely proportional to $C_J$. In order to use this curve...
with confidence, it must represent the highest values $Z_{θJC}$ for each time interval that can be expected from the manufacturing distribution of the products.

While predicting $T_J$ in response to a series of power pulses becomes very complex, superposition of power pulses offers a rigorous numerical method of using the transient thermal resistance curve to secure a solution. Superposition tests the response of a network to any input function by replacing the input with an equivalent series of superimposed positive and negative step functions. Each step function must start from zero and continue to the time for which $T_J$ is to be computed. For example, Figure 13 illustrates a typical train of heating pulses.

$$T_J(t) = T_J(0) + \sum P_i \times [Z_{θJC}(t_n - t_i) - Z_{θJC}(t_n - t_i + 1)]$$

The typical use condition is to compute the peak junction temperature at thermal equilibrium for a train of equal amplitude power pulses as shown in Figure 14.
To further simplify this calculation, the bracketed expression in equation (G) has been plotted for all Fairchild Semiconductor Power MOSFETs, as exemplified by the plot of $Z_{θJC}$ in Figure 14b. From this curve, one can readily calculate $T_J$ if one knows $P_M$, $Z_{θJC}$ and $T_C$ using the expression:

$$T_J = T_C + P_M \times Z_{θJC}$$  \hspace{1cm} (8)

Example: Compute the maximum junction temperature for a train of 1W, 10ms wide heating pulses repeated every 100ms. Assume a case temperature of 55°C.

Duty factor=0.1

From Figure 14b: $Z_{θJC} = 0.14 \times 250°C/W = 35°C/W$

Substituting into Equation (7):

$$T_{J(max)} = 55 + 1 \times 35 = 90°C$$

SAFE OPERATING AREA

The Power MOSFET is not subjected to forward or reverse bias second breakdown, which can easily occur in transistors. Second breakdown is a potentially catastrophic condition in transisors caused by thermal hot spots in the silicon as the transistor turns on or off. However in the MOSFET, the carriers travel through the device much as if it were a bulk semiconductor, which exhibits positive temperature coefficient. If current attempts to self-constrict to a localized area, the increasing temperature of the spot will raise the spot resistance due to positive temperature coefficient of the bulk silicon. The ensuing higher voltage drop will tend to redistribute the current away from the hot spot. Figure 15 shows the safe operating area of the Fairchild Semiconductor Supersot™ NDS351N device.
Note that the safe area boundaries are only thermally limited and exhibit no derating for second breakdown. This shows that while the MOSFET transistor is very rugged, it may still be destroyed thermally by forcing it to dissipate too much power.

**ON-RESISTANCE $R_{DS(on)}$**

The on-resistance of a Power MOSFET is a very important parameter because it determines how much current the device can carry for low to medium frequency (less than 200kHz) applications. After being turned on, the on-state is defined simply as its on-state voltage divided by on-state current. When conducting current as a switch, the conduction losses $P$ are:

$$P_C = I^2_{D(RMS)} \times R_{DS(ON)}$$  \hspace{1cm} (9)

To minimize $R_{DS(on)}$, the applied gate signal should be large enough to maintain operation in the linear or ohmic region as shown in Figure 8. Fairchild Semiconductor SUPERSOT™-3 NDS351N will conduct its rated current for $V_{GS}=4.5$V, which is also the value used to generate the curves of $R_{DS(on)}$ vs $I_D$ and $T_J$ that are shown in Figure 16 for the Fairchild Semiconductor Supersot NDS351N. Since $R_{DS(on)}$ is a function of $T_J$, Figure 16 plots this parameter at varies junction temperatures. Note that as the drain current rises, $R_{DS(on)}$ increases once $I_D$ exceeds the rated current value. Because the MOSFET is a majority carrier device, the component of $R_{DS(on)}$ due to the bulk resistance of the N- silicon in the drain region increases with temperature as well. While this must be taken into account to avoid thermal runaway, it does facilitate parallel operation of MOSFETs. Any imbalance between MOSFETs does not result in current hogging because the device with the most current heat up and ensuing higher on-voltage will divert some current to the other devices in parallel.

![Figure 16. $R_{DS(on)}$ of NDS351N](image)

**TRANSCONDUCTANCE**

Since MOSFETs are voltage controlled, it has become necessary to resurrect the term transconductance $g_{FS}$, commonly used in the past with electron tubes. Referring to Figure 8, $g_{FS}$ equals to the change in drain current divided by the change in gate voltage for a constant drain voltage. Mathematically:

$$g_{FS}(Siemens) = \frac{dl_{D(A)}}{dV_{GST(V)}}$$  \hspace{1cm} (10)
Transconductance varies with operating conditions, starting at 0 for $V_{GS} < V_{GS(th)}$ and peaking at a finite value when the device is fully saturated. It is very small in the ohmic region because the device cannot conduct any more current. Transconductance is useful in designing linear amplifiers and does not have any significance in switching power supplies.

**GATE DRIVE CIRCUITS FOR POWER MOSFETs**

The drive circuit for a Power MOSFET will affect its switching behavior and its power dissipation. Consequently, the type of drive circuitry depends upon the application. If on-state power losses due to $R_{DS(on)}$ will predominate, there is little point in designing a costly drive circuit. This power dissipation is relatively independent of gate drive as long as the gate-source voltage exceeds the threshold voltage by several volts and an elaborate drive circuit to decrease switching times will only create additional EMI and voltage ringing. In contrast, the drive circuit for a device switching at 200KHz or more will affect the power dissipation since switching losses are a significant part of the total power dissipation.

Compare to a junction transistor, the switching losses in a MOSFET can be made much smaller but these losses must still be taken into consideration. Examples of several typical loads along with the idealized switching waveforms and expressions for power dissipation are given in Figure 17 to 19.

Their power losses can be calculated from the general expression:

$$P_D = \frac{1}{2} \int I_D(t) \times V_{DS}(t) dt \times f_S$$  (11)

where $f_S =$ Switching frequency.

For the idealized waveforms shown in the figures, the integration can be approximated by the calculating areas of triangles:

Resistive loads:

$$P_D = \frac{V_{DS}^2}{R} \left[ \frac{t_{on} + t_{off}}{2} + R_{DS(on)} \times T \right] \times f_S$$

Inductive Load:

$$P_D = \frac{V_{CL} \times I_{on} \times (t_{off}^2)}{2} + P_C$$

where $P_C =$ conduction loss during period $T$. 
Capacitive load:

\[ P_D = \left( \frac{C_i V_{DD}^2}{2} + \frac{V_{DD}^2 R_{DS(on)}}{R^2} \times T \right) \times f_S \]

Gate losses and blocking losses can usually be neglected. Using these equations, circuit designer is able to estimate the required heat sink. A final heat run in a controlled temperature environment is necessary to ensure thermal stability.

Since a MOSFET is essentially voltage controlled, the only gate current required is that necessary to charge the input capacitance \( C_{iss} \). In contrast to a 10A transistor, which may require a base current of 2A to ensure saturation, a Power MOSFET can be driven directly by CMOS or open-collector TTL logic circuit similar to that in Figure 20.

Turn-on speed depends upon the selection of resistor \( R_1 \), whose minimum value will be determined by the current sinking rating of the IC. It is essential that an open collector TTL buffer be used since the voltage applied to the gate must exceed the MOSFET threshold voltage. CMOS devices can be used to drive the power device directly since they are capable of operating 15V supplies.

Interface ICs, originally intended for other applications, can be used to drive the Power MOSFETs, as shown below in Figure 21.
Most frequently, switching power supply applications employ a pulse width modulator IC with an NPN transistor output stage. This output transistor is ON when the MOSFET should be ON, hence the type of drive used with open-collector TTL devices cannot be used. Figures 22 and 23 give examples of typical drive circuits used with PWM ICs.

Isolation: Off-line switching power supplies use power MOSFETs in a half bridge configuration because inexpensive, high voltage devices with low $R_{DS(on)}$ are not available.

Since one of the power devices is connected to the positive rail, its drive circuitry is also floating at a high potential. The most versatile method of coupling the drive circuitry is to use a pulse transformer. Pulse transformers are also normally used to isolate the logic circuitry from the MOSFETs operating at high voltage to protect it from a MOSFET failure.

The zener diodes shown in Figure 25 is included to reset the pulse transformer quickly. The duty cycle can approach 50% with a 12V zener diode. For better performance at turn-off, a PNP transistor can be added as shown in Figure 26.

Figure 27 illustrates an alternate method to reverse bias the MOSFET during turn-off by inserting a capacitor in series with the pulse transformer. The capacitor also ensures that the pulse transformer will not saturate due to DC bias.
Opto-isolators may also be used to drive power MOSFETs but their long switching times make them suitable only for low frequency applications.

SELECTING A DRIVE CIRCUIT

Any of the circuits shown are capable of turning a Power MOSFET on and off. The type of circuit depends upon the application. The current sinking and sourcing capabilities of the drive circuit will determine the switching time and switching losses of the power device. As a rule, the higher the gate current at turn-on and turn-off, the lower the switching losses will be. However, fast drive circuits may produce ringing in the gate circuit and drain circuits. At turn-on, ringing in the gate circuit may produce a voltage transient in excess of the maximum $V_{GS}$ rating, which will puncture the gate oxide and destroy it. To prevent this occurrence, a zener diode of appropriate value may be added to the circuit as shown in Figure 28. Note that the zener should be mounted as close as possible to the device.

At turn-off, the gate voltage may ring back up to the threshold voltage and turn on the device for a short period. There is also the possibility that the drain-source voltage will exceed its maximum rated voltage due to ringing in the drain circuit. A protective RC snubber circuit or zener diode may be added to limit drain voltage to a safe level.
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PRODUCT STATUS DEFINITIONS

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In uninterruptable power supplies demands for current handling capability to meet load current in uninterruptable power supplies demands for current handling capability to meet load current requirements plus margins for overload and reliability purposes often exceed the capability of the largest semiconductor device type considered and paralleling may become an attractive alternative. All switching power semiconductors starting with SCR’s [1], bipolar transistors [2-4], darlontons [5], and field effect transistors [6-10], have been successfully paralleled, but proper precaution had to be taken. We will review some of these methods, describe the characteristics of the insulated gate transistors, and show the proper methods to operate this relatively new family of devices in parallel.

All semiconductor circuits using parallel connected devices to switch a higher load current can easily be analyzed by using Kirchhoff’s law. As long as all voltage drops in the parallel branches are equal, the currents through the branches are equal.

This sounds sensible and logical, but as soon as we consider the different stages every switching device has to assume and we consider the parameters of each switching device which guarantees equal voltage drops in the branches over the required temperature range and over the duration of the switching cycle, complications begin to appear.

At first glance, each switching device has only two functional states, an “off-state” and an “on-state”. But by closer examination, we have to consider how we get from “off” to “on” and back to “off”, the “dynamic” area of the switching waveform (Figure 1). The dynamic area is only a fraction of the total waveform, but it is by far the most important when it comes to parallel operation.

In power electronics, there are three different load types; resistive, capacitive, and inductive. The resulting waveforms are sufficiently different to require either different switching devices or the circuit designer may have to change the switching circuit to meet the different requirements, especially when devices are operated in parallel.

Off-State

The off-state is probably the least demanding state in parallel operation of semiconductor devices. As long as leakage current is low, even differences of more than 100% would not create any difficulties.

On-State

The on-state is again a relatively uncritical and uneventful period (Figure 2). Most devices in switching applications are overdriven and differences in gain or transconductance do not translate into proportional output current.

Even if a bipolar device takes a larger share of the total current, the rapid fall-off in gain and the increase in $V_{SAT}$ as it takes the higher share will prevent disaster. Thermal runaway in bipolar applications is not as frequent as we may believe [2-4].

For bipolar devices, the parameter having a clear negative temperature coefficient is $V_{BE}$. $V_{CE(SAT)}$, on the other hand, can have positive or negative temperature coefficient depending on the device type (nnp or pnp) and operating point.

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**Figure 1. Switching Waveform Definitions**

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The ease of paralleling of power FETs has been pointed out by many authors [6-9], and has been demonstrated in many applications, although each application requires analysis of both dynamic and static sharing.

**FIGURE 2. ON TIME OF SWITCHING WAVEFORM AND CONTROLLING PARAMETERS**

**Turn-On Delay Time**

Turn-on delay time is the time from where the control signal is applied, reaches 10% amplitude, to the point where the switched current rises to the 10% amplitude (Figure 3).

Fortunately, differences in turn-on delay are relatively small. Although this delay is significant in large-area SCR's, but it is much less a problem with bipolars or power FET's. It is less important when switching inductive loads, but should be monitored when devices to be paralleled switch resistive load, discharge capacitor or have to carry the recovery current of a diode.

Needless to say, it is desirable to have small turn-on delays for parallel operation. To reduce deltas in tD(ON), it is advisable to drive devices with fast rising control signals and use devices from the same mask design. The same device type number does not guarantee that they are made from the same mask design. Therefore, devices from different manufacturers should not be intermixed.

**Rise Time**

Rise time is an interesting part of the switching waveform (Figure 4). The device operates in an analog domain, although for a very short time, but nevertheless, analog.

Again, transconductance and junction temperature become important considerations, but junction temperature differences as a result of rise time differences are relatively small. Inductors inserted into the emitter lead on bipolars, source lead on FET's or cathode lead on diodes, can be extremely effective [3]. All differences in turn-on delay and rise time become visible at thin part of the waveform. Differences which may exist, although small, require the evaluation of the forward biased safe operating area (FBSOA).

In most cases, transistors have almost rectangular FBSOA for the short durations they remain in the analog domain of the turn-on period. Problems seldom exist, but precautions should not be ignored either.

Note that the device with the shortest turn-on delay and the shortest rise-time will take most of the current. Most transistors have a negative temperature coefficient of input voltage and Miller effect feedback which can cause current begging if power dissipation is high during turn on.

**Turn-Off Delay Time (Storage Time)**

Turn-off delay time is the prelude to the most important part of the switching waveform, especially on bipolar devices (Figure 5). On bipolar devices, it is important to remove the stored charge as fast as possible, which may require more expensive drive circuitry. Especially on large power darlington devices, negative bias or baker clamps result in significant reduction of storage time and improve parallel operations. The transition time of the base current signal from positive to negative (nnp device) is important in the removal rate of the stored charge.
FIGURE 5. TURN-OFF WAVEFORM AND PARAMETERS INFLUENCING IT

Fall Time

Parameters which reduce storage time will also reduce fall time (Figure 6). For paralleled devices, differences in turn-off delay or storage time will have a noticeable effect on fall time.

When inductive loads are turned off, the reverse biased safe operating area (RBSOA) must be considered on bipolar devices. Hot spot formation [11] which results in sudden reduction of the $V_{BE}$ and further increase in $I_B$ could result in permanent damage.

FIGURE 6. FALL TIME AND INFLUENCING PARAMETERS

The Insulated Gate Transistor

The insulated gate transistor (IGT) combines the high input impedance, voltage controlled turn on/turn off capabilities of power MOSFETs and the low on-state conduction losses of bipolar transistors, making it an ideal device for many power electronics switching control applications.

FIGURE 7. UNIT CELL CROSS SECTION AND STEADY STATE EQUIVALENT CIRCUIT OF IGT TRANSISTOR.

In normal operation, the emitter is grounded, the collector biased positive and with no gate-emitter voltage applied; $J_1$ is reverse biased. The device is in the forward blocking mode. When a positive voltage is applied to the gate with respect to the emitter, an inversion channel is formed under the gate and MOSFET current flows from the n+ source region into the n-epi-layer to become the base current for the pnp. Junction $J_2$ becomes forward biased and the device enters the conduction state. Holes are injected from the bot-
tom percent region into the n-epi-layer. The injected minority carrier density is 100 to 1000 times higher than the doping level of the n-type epi-region. This conductivity modulation allows the IGT to operate at a forward conduction current density 20 times that of an equivalent MOSFET. It is primarily in the thick epi, high-voltage devices where conductivity modulation has its major impact to reduce on-resistance.

The typical output characteristics and the symbol of the IGT are shown in Figure 8. Like on MOSFETs, the output characteristics curves are generated by plotting collector emitter currents, collector emitter voltage. Unlike the MOSFET, there is an offset voltage generated by the collector emitter junction of the nnpn-transistor. However, once this offset is overcome, the effective on-resistance in the saturation region is much lower for the IGT than for the MOSET.

**FIGURE 8. OUTPUT CHARACTERISTICS AND CIRCUIT SYMBOL FOR N-CHANNEL IGT TRANSISTOR**

### References


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Rev. H5
An IGT’s few input requirements and low On-state resistance simplify drive circuitry and increase power efficiency in motor-control applications. The voltage-controlled, MOSFET-like input and transfer characteristics of the insulated-gate transistor (IGT) (see EDN, September 29, 1983, pg 153 for IGT details) simplify power-control circuitry when compared with bipolar devices. Moreover, the IGT has an input capacitance mirroring that of a MOSFET that has only one-third the power-handling capability. These attributes allow you to design simple, low-power gate-drive circuits using isolated or level-shifting techniques. What’s more, the drive circuit can control the IGT’s switching times to suppress EMI, reduce oscillation and noise, and eliminate the need for snubber networks.

Use Optoisolation To Avoid Ground Loops

The gate-drive techniques described in the following sections illustrate the economy and flexibility the IGT brings to power control: economy, because you can drive the device’s gate directly from a preceding collector, via a resistor network, for example; flexibility, because you can choose the drive circuit’s impedance to yield a desired turn-off time, or you can use a switchable impedance that causes the IGT to act as a charge-controlled device requiring less than 10 nanocoulombs of drive charge for full turn-on.

Take Some Driving Lessons

Note the IGT’s straightforward drive compatibility with CMOS, NMOS and open-collector TTL/HTL logic circuits in the common-emitter configuration Figure 1A. R3 controls the turn-off time, and the sum of R3 and the parallel combination of R1 and R2 sets the turn-on time. Drive-circuit requirements, however, are more complex in the common-collector configuration Figure 1B.

In this floating-gate-supply floating-control drive scheme, R1 controls the gate supply’s power loss, R2 governs the turn-off time, and the sum of R1 and R2 sets the turn-on time. Figure 1C shows another common-collector configuration employing a bootstrapped gate supply. In this configuration, R3 defines the turn-off time, while the sum of R2 and R3 controls the turn-on time. Note that the gate’s very low leakage allows the use of low-consumption bootstrap supplies using very low-value capacitors. Figure 1 shows two of an IGT’s strong points. In the common-emitter Figure 1A, TTL or MOS-logic circuits can drive the device directly. In the common-collector mode, you’ll need level shifting, using either a second power supply Figure 1B or a bootstrapping scheme Figure 1C.

In the common-collector circuits, power-switch current flowing through the logic circuit’s ground can create problems. Optoisolation can solve this problem (Figure 2A.) Because of the high common-mode dV/dt possible in this configuration, you should use an optoisolator with very low isolation capacitance; the H11AV specs 0.5pF maximum.
For optically isolated “relay-action” switching, it makes sense to replace the phototransistor optocoupler with an H11L1 Schmitt-trigger optocoupler (Figure 2B). For applications requiring extremely high isolation, you can use an optical fiber to provide the signal to the gate-control photodetector. These circuit examples use a gate-discharge resistor to control the IGT’s turn-off time. To exploit fully the IGT’s safe operating area (SOA), this resistor allows time for the device’s minority carriers to recombine. Furthermore, the recombination occurs without any current crowding that could cause hot-spot formation or latch-up pn-pn action. For very fast turn-off, you can use a minimal snubber network, which allows the safe use of lower value gate resistors and higher collector currents.

Available photovoltaic couplers have an output-current capability of approximately 100µA. Combined with approximately 100kΩ equivalent shunt impedance and the IGT’s input capacitance, this current level yields very long switching times. These transition times (typically ranging to 1 msec) vary with the photovoltaic coupler’s drive current and the IGT’s Miller-effect equivalent capacitance.

Figure 3 illustrates a typical photovoltaic-coupler drive along with its transient response. In some applications, the photovoltaic element can charge a storage capacitor that’s subsequently switched with a phototransistor isolator. This isolator technique - similar to that used in bootstrap circuits provides rapid turn-on and turn-off while maintaining small size, good isolation and low cost.

In common-collector applications involving high-voltage, reactive-load switching, capacitive currents in the low-level logic circuits can flow through the isolation capacitance of the control element (eg, a pulse transformer, optoisolator, piezoelectric coupler or level-shift transistor). These currents can cause undesirable effects in the logic circuitry, especially in high-impedance, low-signal-level CMOS circuits.

The solution? Use fiber-optic components Figure 4 to eliminate the problems completely. As an added feature, this low-cost technique provides physical separation between the power and logic circuitry, thereby eliminating the effects of radiated EMI and high-flux magnetic fields typically found near power-switching circuits. You could use this method with a bootstrap-supply circuit, although the fiber-optic system’s reduced transmission efficiency could require a gain/speed trade-off. The added bipolar signal transistor minimizes the potential for compromise.

**Pulse-Transformer Drive Is Cheap And Efficient**

Photovoltaic couplers provide yet another means of driving the IGT. Typically, these devices contain an array of small silicon photovoltaic cells, illuminated by an infrared diode through a transparent dielectric. The photovoltaic coupler provides an isolated, controlled, remote dc supply without the need for oscillators, rectifiers or filters. What’s more, you can drive it directly from TTL levels, thanks to its 1.2V, 20mA input parameters.

FIGURE 2A. AVOID GROUND-LOOP PROBLEMS BY USING AN OPTOISOLATOR. THE ISOLATOR IGNORES SYSTEM GROUND CURRENTS AND ALSO PROVIDES HIGH COMMON-MODE RANGE.

FIGURE 2B. A SCHMITT-TRIGGER OPTOISOLATOR YIELDS “SNAP-ACTION” TRIGGERING SIMILAR TO THAT OF A RELAY.

FIGURE 3. AS ANOTHER OPTICAL-DRIVE OPTION, A PHOTOVOLTAIC COUPLER PROVIDES AN ISOLATED, REMOTE DC SUPPLY TO THE IGT’S INPUT. ITS LOW 100µA OUTPUT, HOWEVER, YIELDS LONG IGT TURN-ON AND TURN-OFF TIMES.
FIGURE 5A. YIELDING 4-kV ISOLATION, A PIEZOELECTRIC COUPLER PROVIDES TRANSFORMER-LIKE PERFORMANCE AND AN ISOLATED POWER SUPPLY.

FIGURE 5B. THIS CIRCUIT PROVIDES THE DRIVE FOR THIS ARTICLE’S MOTOR-CONTROL CIRCUIT.
A piezoelectric coupler operationally similar to a pulse-train drive transformer, but potentially less costly in high volume is a small, efficient device with isolation capability ranging to 4kV. What’s more, unlike optocouplers, they require no auxiliary power supply. The piezo element is a ceramic component in which electrical energy is converted to mechanical energy, transmitted as an acoustic wave, and then reconverted to electrical energy at the output terminals Figure 5A.

The piezo element’s maximum coupling efficiency occurs at its resonant frequency, so the control oscillator must operate at that frequency. For example, the PZT61343 piezo coupler in Figure 5B’s driver circuit requires a 108kHz, ±1%-accurate astable multivibrator to maximize mechanical oscillations in the ceramic material. This piezo element has a 1W max power handling capability and a 30mA p-p max secondary current rating. The 555 timer shown provides compatible waveforms while the RC network sets the frequency.

Isolate With Galvanic Impunity

Do you require tried and true isolation? Then use transformers; the IGT’s low gate requirements simplify the design of independent, transformer-coupled gate-drive supplies. The supplies can directly drive the gate and its discharge resistor Figure 6, or they can simply replace the level-shifting supplies of Figure 2. It’s good practice to use pulse transformers in drive circuitry, both for IGT’s and MOSFETs, because these components are economical, rugged and highly reliable.

![Figure 6A](image1)

**FIGURE 6A. PROVIDING HIGH ISOLATION AT LOW COST, PULSE TRANSFORMERS ARE IDEAL FOR DRIVING THE IGT. AT SUFFICIENTLY HIGH FREQUENCIES, C1 CAN BE THE IGT’S GATE-EMITTCAPACITANCE ALONE.**

![Figure 6B](image2)

**FIGURE 6B. A HIGH-FREQUENCY OSCILLATOR IN THE TRANSFORMER’S PRIMARY YIELDS UNLIMITED ON-TIME CAPABILITY.**

In the pulse-on, pulse-off method Figure 6A, C1 stores a positive pulse, holding the IGT on. At moderate frequencies (several hundred Hertz and above), the gate-emitter capacitance alone can store enough energy to keep the IGT on; lower frequencies require an additional external capacitor. Use of the common-base n-p-n bipolar transistor to discharge the capacitance minimizes circuit loading on the capacitor. This action extends continuous on-time capability without capacitor refreshing; it also controls the gate-discharge time via the 1kΩ emitter resistor.

![Figure 8](image3)

**FIGURE 8. THIS 6-STEP 3-PHASE-MOTOR DRIVE USES THE IGT-DRIVE TECHNIQUES DESCRIBED IN THE TEXT. THE REGULATOR ADJUSTS THE OUTPUT DEVICES’ INPUT LEVELS; THE VOLTAGE-CONTROLLED OSCILLATOR VARIES THE SWITCHING FREQUENCY AND ALSO PROVIDES THE CLOCK FOR THE 3-PHASE TIMING LOGIC. THE V/F RATIO STAYS CONSTANT TO MAINTAIN CONSTANT TORQUE REGARDLESS OF SPEED.**
Piezoelectric Couplers Provide 4-kV Isolation

Using a high-frequency oscillator for pulse-train drive Figure 6B yields unlimited on-time capability. However, the scheme requires an oscillator that can be turned on and off by the control logic. A diode or zener clamp across the transformer’s primary will limit leakage-inductance flyback effects. To optimize transformer efficiency, make the pulses’ voltage x time products equal for both the On and the Off pulses. In situations where the line voltage generates the drive power, a simple relaxation oscillator using a programable unijunction transistor can derive its power directly from the line to provide a pulse train to the IGT gate.

The circuit shown in Figure 7 accommodates applications involving lower frequencies (a few hundred Hertz and below). The high oscillator frequency (greater than 20kHz) helps keep the pulse transformer reasonably small. The voltage-doubler circuitry improves the turn-on time and also provides long on-time capability. Although this design uses only a 5V supply on the primary side of a standard trigger transformer, it provides 15V gate-to-emitter voltage.
Polyphase motors, controlled by solid-state, adjustable-frequency ac drives, are used extensively in pumps, conveyors, mills, machine tools and robotics applications. The specific control method could be either 6-step or pulse-width modulation. This section describes a 6-step drive that uses some of the previously discussed drive techniques (see page 11, “Latch-Up: Hints, Kinks and Caveats”).

Figure 8 defines the drive’s block diagram. A 3-phase rectifier converts the 220V ac to dc; the switching regulator varies the output voltage to the IGT inverter. At the regulator’s output, a large filter capacitor provides a stiff voltage supply to the inverter.

The motor used in this example has a low slip characteristic and is therefore very efficient. You can change the motor’s speed by varying the inverter’s frequency. As the frequency increases, however, the motor’s air-gap flux diminishes, reducing developed-torque capability. You can maintain the flux at a constant level (as in a dc shunt motor) if you also vary the voltage so the V/F ratio remains constant.

Fiber-Optic Drive Eliminates Interference

In the example given, the switching regulator varies the IGT inverter’s output by controlling its dc input; the voltage-controlled oscillator (VCO) adjusts the inverter’s switching frequency, thereby varying the output frequency. The VCO also drives the 3-phase logic that provides properly timed pulsed outputs to the piezo couplers that directly drive the IGT.

Sensing the dc current in the negative rail and inhibiting the gate signal protect the IGT from overload and shoot-through (simultaneous conduction) conditions. If a fault continues to exist for an appreciable period, inhibiting the switching regulator causes the inverter to shut off. The inverter’s power-output circuit is shown in Figure 9A; the corresponding timing diagrams show resistive-load current waveforms that indicate the 3-phase power Figure 9B and waveforms of the output line voltage and current Figure 9C.

In Figure 9’s circuit, it appears that IGTs Q1 through Q6 will conduct for 180°. However, in a practical situation, it’s necessary to provide some time delay (typically 10° to 15°×) during the positive-to-negative transition periods in the phase current. This delay allows the complementary IGTs to turn off before their opposite members turn on, thus preventing cross conduction and eventual destruction of the IGTs.

Because of the time delay, the maximum conduction time is 165° of every 360° period. Because the IGTs don’t have an integral diode, it’s necessary to connect an antiparallel diode externally to allow the freewheeling current to flow. Inductor L1 limits the di/dt during fault conditions; freewheeling diode D7 clamps the IGT’s collector supply to the dc bus.

The peak full-load line current specified by the motor manufacturer determines the maximum steady-state current that each transistor must switch. You must convert this RMS-specified current to peak values to specify the proper IGT. If the input voltage regulator had a fixed output voltage and a constant frequency, each IGT would be required to supply the starting locked-rotor current to the motor. This current could be as much as 15 times the full-load running current.

**FIGURE 10A. COMPONENT SELECTION IS IMPORTANT. THE IGT SELECTED CIRCUIT HANDLES 10A, 500V AT 150°C. THE ANTI-PARALLEL DIODES HAVE A SIMILAR CURRENT RATING.**

**FIGURE 10B. SELECT R TO YIELD THE DESIRED TURN-OFF TIME. FINALLY, L1’S VALUE DETERMINES THE FAULT-CONDITION ACTION TIME.**
It’s impractical, however, to rate an inverter based on locked-rotor current. You can avoid this necessity by adjusting the switching regulator’s output voltage and by providing a fixed output-current limit slightly higher than the maximum full-load current. This way, the current requirements during start-up will never exceed the current capability of an efficiently sized inverter.

For example, consider a 2-hp, 3-phase induction motor specifying $V_L$ at 230V RMS and full-load current ($I_{LFL}$) at 6.2A RMS. For the peak current of 8.766A, you can select IGT type D94FR4. This device has a reverse-breakdown SOA (RBSOA) of 10A, 500V for a clamped inductive load at a junction temperature of 150°C. A 400V IGT could also do the job, but the 500V choice gives an additional derating safety margin. You must set the current limit at 9A to limit the inrush current during start-up. Note that thanks to the IGT’s adequate RBSOA, you don’t need turn-off snubbers.

**FIGURE 11A.** PROVIDING PROPERLY TIMED DRIVE TO THE IGTS, THE CIRCUIT USES PIEZO COUPLING TO THE UPPER POWER DEVICE. THE 3-TRANSISTOR DELAY CIRCUIT PROVIDES THE NEEDED 15° LAG TO THE LOWER IGT TO AVOID CROSS CONDUCTION.

**FIGURE 11B.** THE TIMING DIAGRAM SHOWS THE 555’S 108-KHz DRIVE TO THE PIEZO DEVICE AND THE LATTER’S SLOW RESPONSE.
Use 6-Step Drive For Speed-Invariant Torque

Figure 10A shows the inverter circuit configured for this example. Diodes D1 through D6 carry the same peak current as the IGTs; consequently, they’re rated to handle peak currents of at least 8.766A. However, they only conduct for a short time (15° to 20° of 180°), so their average-current requirement is relatively small.

External circuitry can control the IGT’s current fall time. Resistor R controls tF1 Figure 10B; there’s no way to control tF2, an inherent characteristic of the selected IGT. In this example, a 4.7-kΩ gate-to-emitter resistor provides the appropriate fall time. The choice of current-limiting inductor L1 is based on the IGT’s overload-current rating and the action time (the sum of the sensor’s sensing and response time and the IGT’s turn-off time) in fault conditions.

You could use a set of flip flops and a multivibrator to generate the necessary drive pulses and the corresponding 120° delay between the three phases in Figure 10’s circuit. A voltage-controlled oscillator serves to change the inverter’s output frequency. In this circuit, IGTs Q1, Q3 and Q5 require isolated gate drive; the drive for Q2, Q4 and Q6 can be referred to common. If you use optocouplers for isolation, you’ll need three isolated or bootstrap power supplies (in addition to the 5V and 24V power supplies) to drive the IGTs. Another alternative is to use transformer coupling.

165° Conduction Prevents Shoot-Through

Consider, however, using Figure 11A’s novel, low-cost circuit. It uses a piezo coupler to drive the isolated IGT. As noted, the coupler needs a high-frequency square wave to induce mechanical oscillations in its primary side. The 555 oscillator provides the necessary 108-kHz waveform; its output is gated according to the required timing logic and then applied to the piezo coupler’s primary. The coupler's rectified output drives the IGT’s gate; the 4.7kΩ gate-to-emitter resistor provides a discharge path for CGE during the IGT’s turn-off. The circuit’s logic-timing diagram is shown in Figure 11B.

The piezo coupler’s slow response time Figure 12A contributes approximately 2° to the 15° to 20° turn-on/tturn-off delay needed to avoid shoot-through in the complementary pairs. The corresponding collector current is shown in Figure 12B. C1 and its associated circuitry provide the remaining delay as follows:

---

**FIGURE 12A.** THE PIEZO COUPLER'S SLOW RESPONSE IS NOT A DISADVANTAGE IN THIS ARTICLE’S CIRCUIT. IN FACT, IT CONTRIBUTES 2° TO THE REQUIRED 15° TURN-ON/TURN-OFF DELAY.

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**FIGURE 12B.** THE DRIVEN IGT’S COLLECTOR CURRENT IS SHOWN

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When Q3’s base swings negative, C1 - at this time discharged - turns on Q5. Once C1 is charged, Q5 turns off, allowing a drive pulse to turn the IGT on. When Q7’s base goes to ground, Q4 turns on and discharges C1, initiating the IGT’s turn-off. Figure 13 shows the motor current and corresponding line voltage under light-load Figure 12A and full-load Figure 12B conditions.

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To complete the design of the 6-step motor drive, it's necessary to consider protection circuitry for the output IGTs. The drive receives its power from a switching supply already containing provisions for protection from line over-voltage and under-voltage and transient effects. However, you still have to guard the power switches against unwanted effects on the output lines and the possibility of noise or other extraneous signals causing gate-drive timing errors.

The best protection circuit must match the characteristics of the power switch and the circuit's bias conditions. The IGT is very rugged during turn-on and conduction, but it requires time to dissipate minority carriers when turning off high currents and voltages. An analysis of the possible malfunction condition.

FIGURE 14. THE LOWEST COST SENSOR IMAGINABLE, A PIECE OF COPPER WIRE SERVES AS THE CURRENT MONITOR IN THIS SYSTEM. THE CHOPPED AND AMPLIFIED VOLTAGE DROP ACROSS THE WIRE TRIGGERS A GATE-DRIVE SHUT-OFF CIRCUIT UNDER FAULT CONDITIONS.
**FIGURE 15A.** This all-encompassing protection system provides three independent shutdown functions - one each for the upper and lower IGTs and the high-voltage supply.

**FIGURE 15B.** This circuit provides chopper drive for the copper-wire sensor in Figure 15A.

**FIGURE 15C.** Shows the high-voltage shutdown circuit.
Latch-Up: Hints, Kinks and Caveats

The IGT is a rugged device, requiring no snubber network when operating within its published safe-operating-area (SOA) ratings. Within the SOA, the gate emitter voltage controls the collector current. In fact, the IGT can conduct three to four times the published maximum current if it’s in the ON state and the junction temperature is +150°C maximum.

However, if the current exceeds the rated maximum, the IGT could lose gate control and latch up during turn-off attempts. The culprit is the parasitic SCR formed by the pnpn structure shown in Figure 16. In the equivalent circuit, Q1 is a power MOSFET with a normal parasitic transistor (Q2) whose base-emitter junction is shunted by the low-value resistance R1.

For large current overloads, the current flowing through R1 can provoke SCR triggering. In the simplest terms, R1 represents the equivalent of a distributed resistor network, whose magnitude is a function of Q2’s VCE. During normal IGT operation, a positive gate voltage (greater than the threshold) applied between Q1’s gate and source turns the FET on. The FET then turns on Q3 (a pnp transistor with very low gain), causing a small portion of the total collector current to flow through the R1 network.

To turn the IGT off, you must reduce the gate-to-emitter voltage to zero. This turns Q1 off, thus initiating the turn-off sequence within the device. Total fall time includes current-fall-time one (tF1) and current-fall-time two (tF2) components. The turn-off is a function of the gate-emitter resistance, Q3’s storage time and the value of VGE prior to turn-off. Device characteristics fix both the delay time and the fall time.

Forward-Bias Latch-Up

Within the IGT’s current and junction-temperature ratings, current does not flow through Q2 under forward-biased conditions. When the current far exceeds its rated value, the current flow through R1 increases and Q3’s VCE also increases because of MOSFET channel saturation. Once Q3’s IC*R1 drop exceeds Q2’s VBE(ON), Q2 turns on and more current flow bypasses the FET.

The positive feedback thus established causes the device to latch in the forward-biased mode. The value of IC at which the IGT latches on while in forward conduction is typically three to four times the device’s maximum rated collector current. When the collector current drops below the value that provokes Q2 turn-on, normal operation resumes if chip temperature is still within ratings.

If the gate-to-emitter resistance is too low, the Q2-Q3 parasitic SCR can cause the IGT to latch up during turn-off. During this period, RCE determines the drain-source dV/dt of power MOSFET Q1. A low R1 causes a rapid rise in voltage-this increases Q2’s VCE, increasing both R1’s value and Q2’s gain.

Because of storage time, Q3’s collector current continues to flow at a level that’s higher than normal for the FET bias. During rapid turn-off, a portion of this current could flow in Q2’s base-emitter junction, causing Q2 to conduct. This process results in device latch-up; current distribution will probably be less uniform than in the case of forward-bias latch-up.

Because the gains of Q2 and Q3 increase with temperature and VCE, latching current - high at +25°C - decreases as a function of increasing junction temperature for a given gate-to-emitter resistance.

How do you test an IGT’s turn-off latching characteristic? Consider the circuit in Figure 17. Q1’s base-current pulse width is set approximately 2µsec greater than the IGT’s gate-voltage pulse width. This way, the device under test (DUT) can be switched through Q1 when reverse-bias latch-up occurs. This circuit allows you to test an IGT’s latching current nondestructively.

The results? Clamped-inductive-load testing with and without snubbers reveals that snubbing increases current handling dramatically: With RGE = 1kΩ a 0.02µF snubber capacitor increases current capability from 6A to 10A; with RGE = 5kΩ a 0.09µF snubber practically doubles capacity (25A vs 13A).

Conclusions? You can double the IGT’s latching current by increasing RGE from 1kΩ to 5kΩ and double it again with a polarized snubber using CS < 0.1µF. The IGT is therefore useful in situations where the device must conduct currents of five to six times normal levels for short periods.

Finally, you can also use the latching behavior to your advantage under fault conditions. In other words, if the device latches up during turn-off under normal operation, you could arrange it so that a suitable snubber is switched electronically across the IGT.

FIGURE 16. THE IGT’S PARASITIC SCR IS RESPONSIBLE FOR THE DEVICE’S LATCH-UP CHARACTERISTICS.
FIGURE 17. USE THIS LATCHING-CURRENT TESTER TO TEST IGTS NONDESTRUCTIVELY. Q₁’S BASE-DRIVE PULSE WIDTH IS GREATER THAN THAT OF THE IGT’S GATE DRIVE, SO THE IGT UNDER TEST IS SWITCHED THROUGH Q₁ WHEN REVERSE-BIAS LATCH-UP OCCURS.

Q₁ = D66EV7
Q₂ = DUT D94FQ4
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